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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,432	01/23/2004	Paul Brian Ripy	200-66300 (2003-00900)	6824

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,432	RIPY ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,16 and 17* is/are rejected.

7)☒ Claim(s) *4-15 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

2. The IDS filed on 05/18/2005 has been received and carefully considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 16 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Larson et al. (USPN: 5,481,680) hereinafter, Larson.

As per claim 1, Larson teaches a method of adding grant information (i.e. the grant bits, G0-G3 in Fig. 7) to a memory (i.e. the memory device 12 in Fig. 1) having a plurality of physical addresses each physical address identifies an arbitration period, the method comprising the steps of: if grant information is to be added to the memory, determining a number of desired arbitration periods requested by a communication circuit; assigning a range of logical addresses to the communication circuit, the number of logical addresses in the range being equal to the number of desired arbitration periods; and forming a number of physical addresses by changing a number of the logical addresses in the range, each logical address having a corresponding physical address, a number of the physical addresses being spaced apart (i.e. the grant bits G0-G3 in Fig. 7 are assigned to each one of the plurality of logical addresses 0000-1111 of

the memory as shown in Fig. 7 and each logical address corresponds to a physical address of the memory spaced apart from the physical address, which is an inherent feature of the method taught by Larson) (e.g. see Col. 5, lines 30+ and Figs. 1, 5-7).

As per claim 2, Larson teaches the claimed invention as described above and furthermore, Larson teaches that the step of writing grant information (i.e. the grant bits, G0-G3 in Fig. 7) for the communication circuit to the physical addresses that correspond with the logical addresses (i.e. 0000-1111 in Fig. 7) in the range (e.g. see Fig. 7).

As per claim 3, Larson teaches the claimed invention as described above and furthermore, Larson teaches that the memory (i.e. the memory device 12 in Fig. 1) has a logical address that represents a next available arbitration period and the range of logical addresses are sequential (i.e. the logical addresses 0000-1111 are in sequence) (e.g. see Fig. 7).

As per claims 16 and 17, Larson teaches a communications circuit as shown in Fig. 1. A transmit circuit for transmitting information onto a bus; a receive circuit for receiving information from the bus; and a logic circuit are inherently embedded in the CPU 14 shown in Fig. 1. Larson also teaches the further claimed limitations of claim 16 and 17 as shown above in the rejection of claim 1.

Allowable Subject Matter

4. Claims 4, 11, 14-15 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 5-10 would also

be allowable for the same reason(s) as they further limit the objected claim 4. Similarly, claims 12-13 would also be allowable for the same reason(s) as they further limit the objected claim 11; and claim 20 would also be allowable for the same reason(s) as they further limit the objected claim 19.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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MATTHEW D. ANDERSON
PRIMARY EXAMINER